## CLAIMS

What is claimed:

1. A method for forming a plurality of thin-film devices comprising:

providing a flexible substrate; and

utilizing a self-aligned imprint lithography (SAIL) process to form the plurality of thin-film devices on the flexible substrate.

2. The method of claim 1 wherein the plurality of thin-film devices comprises an array of interconnected transistors.

3. The method of claim 1 wherein the SAIL process comprises:

depositing at least one material over the flexible substrate;

forming a 3D structure over the at least one material; and

patterning the at least one material in accordance the desired characteristics of the plurality of thin-film devices.

4. The method of claim 1 wherein utilizing a SAIL process includes:

depositing a planarization material.

5. The method of claim 2 wherein the array of interconnected transistors comprises an active matrix backplane.

6. The method of claim 3 wherein the 3D structure is comprised of an imprint polymer.

7. The method of claim 3 wherein forming a 3D structure over the at least one material comprises:

depositing an imprint polymer over the at least one material; and

forming a 3D pattern in the imprint polymer.

8. The method of claim 3 wherein depositing at least one material over the flexible substrate further comprises:

depositing a buffer layer of material on the flexible substrate;

depositing a layer of Si over the buffer layer;

depositing a dielectric layer over the Si layer; and

depositing a gate metal layer over the dielectric layer.

9. The method of claim 4 wherein the planarization material is at least one of a photo-resist, a UV-curable polymers and a spin-on glass.

10. The method of claim 8 wherein patterning the at least one material comprises:

etching the gate metal layer and the dielectric layer thereby exposing the Si layer;

providing a doped Si layer;

depositing a metal layer;

depositing a planarization material;

removing a portion of the planarization material thereby exposing a portion of the metal layer;

removing the exposed portion of the metal layer thereby exposing a portion of the imprint polymer;

removing a portion of the imprint polymer; and

etching the gate metal layer, the dielectric layer and the Si layer.

11. The method of claim 10 further comprising:

removing the planarization material.

12. The method of claim 10 wherein the planarization material is capable of being selectivity removed with respect to the imprint polymer.

13. The method of claim 10 wherein providing a doped Si layer further comprises:

utilizing a laser doping process to dope the Si layer.

14. The method of claim 10 wherein providing a doped Si layer further comprises:

utilizing a plasma doping process to dope the Si layer.

15. The method of claim 10 wherein providing a doped Si layer further comprises:

depositing a doped layer of Si.

16. The method of claim 10 wherein the step of depositing a planarization material further comprises:

planarizing the planarization material via a chemical-mechanical polishing process.

17. A system for forming a plurality of thin-film devices comprising:

means for utilizing a SAIL process in conjunction with a flexible substrate to

form a plurality of thin-film devices on the flexible substrate.

18. The system of claim 17 wherein the plurality of thin-film devices comprises an array of interconnected transistors.

19. The system of claim 17 wherein the means for utilizing a SAIL process comprises:

means for depositing at least one material over the flexible substrate;

means for forming a 3D structure over the at least one material; and

means for patterning the at least one material in accordance with the desired characteristics of the plurality of thin-film devices.

20. The system of claim 17 wherein the means for utilizing a SAIL process includes:

means for depositing a planarization material.

21. The system of claim 18 wherein the array of interconnected transistors comprises an active matrix backplane.

22. The system of claim 19 wherein the 3D structure is comprised of an imprint polymer.

23. The system of claim 19 wherein the means for forming a 3D structure over the at least one material comprises:

means for depositing an imprint polymer over the at least one material; and

means for forming a 3D pattern in the imprint polymer.

24. The system of claim 19 wherein the means for depositing at least one material over the flexible substrate further comprises:

means for depositing a buffer layer of material on the flexible substrate;

means for depositing a layer of Si over the buffer layer;

means for depositing a dielectric layer over the Si layer; and

means for depositing a gate metal layer over the dielectric layer.

25. The system of claim 20 wherein the planarization material is at least one of a photo-resist, a UV-curable polymers and a spin-on glass.

26. The system of claim 24 wherein the means for patterning the at least one material comprises:

means for etching the gate metal layer and the dielectric layer thereby exposing the Si layer;

means for providing a doped Si layer;

means for depositing a metal layer;

means for depositing a planarization material;

means for removing a portion of the planarization material thereby exposing a portion of the metal layer;

means for removing the exposed portion of the metal layer thereby exposing a portion of the imprint polymer;

means for removing a portion of the imprint polymer; and

means for etching the gate metal layer, the dielectric layer and the Si layer.

27. The system of claim 26 further comprising:

means for removing the planarization material.

28. The system of claim 26 wherein the planarization material is capable of being selectivity removed with respect to the imprint polymer.

29. The system of claim 26 wherein the means for providing a doped Si layer further comprises a laser doping process to dope the Si layer.

30. The system of claim 26 wherein the means for providing a doped Si layer further comprises a plasma doping process to dope the Si layer.

31. The system of claim 26 wherein the means for providing a doped Si layer further comprises:

means for depositing a doped layer of Si.

32. A structure comprising:

a flexible substrate; and

at least two thin-film transistors formed on the flexible substrate the at least two thin-film transistors including an interconnection therebetween wherein the interconnection includes an imprint polymer between a first metal and a second metal.

33. The structure of claim 32 wherein the at least two thin-film transistors comprises an array of interconnected transistors.

34. The structure of claim 33 wherein the array of interconnected transistors comprises an active matrix backplane.

35. The structure of claim 34 wherein the first metal includes a gate metal and the second metal includes a source drain metal.

36. An active matrix backplane comprising:

a flexible substrate; and

an array of interconnected thin-film transistors wherein the array comprises at least two thin-film transistors formed on the flexible substrate, the at least two thin-film transistors including an interconnection therebetween wherein the interconnection includes an imprint polymer between a gate metal and a source drain metal.

37. A method for forming a plurality of thin-film devices comprising:

providing a non-flexible substrate; and

utilizing a self-aligned imprint lithography (SAIL) process to form the plurality of thin-film devices on the non-flexible substrate.